

Abstract of the Disclosure

When first memory cells connected to a bit line are selected, the bit-line sense amplifier amplifies the voltage levels of the bit line and the complementary bit line using the first current path and the second current path, wherein the first current path is
5 formed between the output node of the sensing enable unit and the bit line in response to the voltage level of the complementary bit line and the first addressing signal, and the second current path is formed between the output node of the sensing enable unit and the complementary bit line in response to the voltage level of the bit line and the second
10 addressing signal.

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